

TEXAS







Dileep Bhandarkar, Ph. D. IEEE Fellow

> Computer History Museum 21 August 2014







# Disclaimer

The opinions expressed here are my own and may be a result of the way in which my highly disorganized and somewhat forgetful mind interprets a particular situation or concept.

They are not approved or authorized by my current or past employers, family, or friends.

If any or all of the information or opinions found here does accidentally offend, humiliate or hurt someone's feelings, it is entirely unintentional.

> "Come on the amazing journey And learn all you should know." – The Who

## **The Stops Along My Journey**

- 1970: B. Tech, Electrical Engineering (Distinguished Alumnus)
  Indian Institute of Technology, Bombay
- 1973: PhD in Electrical Engineering
  - Carnegie Mellon University
  - Thesis: Performance Evaluation of Multiprocessor Computer Systems
- 4 years Texas Instruments
  - Research on magnetic bubble & CCD memory, Fault Tolerant DRAM
- 17.5 years Digital Equipment Corporation
  - Processor Architecture and Performance
- 12 years Intel
  - Performance, Architecture, Strategic Planning
- 5.5 years Microsoft
  - Distinguished Engineer, Data Center Hardware Engineering
- Since January 2013 Qualcomm Technologies Inc
  - VP Technology

"Follow the path of the unsafe, independent thinker. Expose your ideas to the danger of controversy. Speak your mind and fear less the label of "crackpot" than the stigma of conformity." – Thomas J. Watson



MOORE'S LAW "Transistor density on integrated circuits doubles about every two years." \*

<b>1950s</b>	1960s	<b>1970s</b>	1980s	<b>1990s</b>	2000s
Silicon	TTL	8-bit	32-bit	32-bit	64-bit
Transistor	Quad Gate	Microprocessor	Microprocessor	Microprocessor	Microprocessor
1	16	4500	275,000	3,100,000	592,000,000
Transistor	Transistors	Transistors	Transistors	Transistors	Transistors

Microelectronic silicon computer "chips" have grown in capability from a single transistor in the 1950s to hundreds of millions of transistors per chip on today's microprocessor and memory devices. From the first documented semiconductor effect in 1833 to the transition from transistors to integrated circuits in the 1960s and 70s, this website explores key milestones in the development of these extraordinary engines that power the computing and communications revolution of the information age. **1958**: Jack Kilby's Integrated Circuit

\*Source: "Moore's Law: Raising the Bar" (Intel Corporation 2005)

Photo credits: Fairchild Camera and Instrument Corporation, Intel Corporation (Note that images are not to scale)

### SSI -> MSI -> LSI -> VLSI -> OMGWLSI



## What is Moore's Law?





# 1971: 4004 Microprocessor



The 4004 was Intel's first microprocessor. This breakthrough invention powered the **Busicom calculator** and paved the way for embedding intelligence in inanimate objects as well as the personal computer.



Introduced November 15, 1971 108 KHz, 50 KIPs , 2300 10μ transistors

# 1971: 1K DRAM



### Intel® 1103 DRAM Memory

- Intel delivered the 1103 to 14 of the 18 leading computer manufacturers.
- Since the production costs of the 1103 were much lower than the costs of a magnetic core memory the market developed rapidly, becoming the world's best selling memory chip and was finally responsible for the obsolescence of magnetic core memory.



### **DRAM Memory Board**

### Core Memory



# IBM 360/67 and Univac 1108 at CMU in 1970

- The S/360-67 operated with a basic internal cycle time of 200 nanoseconds and a basic 750 nanosecond magnetic core storage cycle
- Dynamic Address Translation (DAT) with support for 24 or 32-bit virtual addresses using segment and page tables (up to 16 segments each containing up to 256 x 4096 byte pages)

UNIVAC HIDE



Snow White (IBM) and the Seven Dwarfs (RCA, GE, Burroughs, Univac, NCR, Control Data, Honeywell)

## **DEC PDP-10**



# Sept 1973: Mission Accomplished



Dileap P. Bhardarkar

DEPARTMENT of COMPUTER SCIENCE



Carnegie-Mellon University

Created with RUNOFF (XOFF) and printed on Xerox Graphics Printer prototype connected to a DEC PDP-11/20 running printer software developed by Chuck Geschke.

#### MARKOV CHAIN MODELS FOR ANALYZING MEMORY INTERFERENCE IN MULTIPROCESSOR COMPUTER SYSTEMS

Oleep P. Bhandarkar' Samuel H. Fuller Carnegie-Meloh University Pittsburgh, Permisitvania

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1<sup>st</sup> paper presented at the First Annual Symposium on Computer Architecture (later named ISCA) in Dec 1973 after Opening Keynote by Maurice Wilkes!



# Oct 1973 First Job in Dallas, Texas



# 1973: 4K DRAM

### 22 pin package



TI and Intel used 22 pins for their competing, nextgeneration 4K devices in 1973. But Mostek soon dominated the 4K market by squeezing it into a 16 pin package using an address multiplexing scheme, which was a revolutionary approach that reduced cost and board space. By 1976 everyone adopted Mostek's approach for 16K and larger DRAMs.



### 16 pin package with RAS/CAS

MOSTEK's 16-pin 4K RAM makes memory design easy.



In MUSTERS MADPADP you can duce memory and particular and particular by MUSTERS where the State and particular



Electronic Design June 7, 1974 Pages 31-32

## **Texas Instruments Adventure**

### Magnetic Bubble Memory • Fault Tolerant DRAM •

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#### United States Patent 109 1613 Sept. 6, 1977 Choate et al. 1453 1,841,476 10/2974 [54] FAULT-TOLERANT CILL ADDRESSABLE Bothm 5/1975 1,883,470 Hunter ARRAY 1,897,636 Beautiful Bam Cay Chosts, Dallas; Dil [75] leventors: Primary Exempter-Termil W. Fran kar, Richardson, buth or Attorney, Agent, or Firm-Harold Levice; Janua T. Tes Confort, William E. Hiller [73] Team ABSTRACT Dallas, Tex A small programmable summory means such as an elec-[21] Appl. No.: 592,979 trically programmable logic array is isoperated on the chip of a conventional bit addressable random ac-1221 Filed: July 3, 1975 cess memory or other cell addressable array circuit GHC II/40: GHC 13/00 Int. CU The array has one or more superflamas rows and/or 340/173 R; 340/173 BB; T15. CL columns of cells held in reserve. Processing and testing 344/98 of the chip is conducted is a conventional manuer 340/175 R. 173 BB, 172.5 1583 Chips with faulty cells are corrected by program the exempty means with the cell addresses of the faulty Raterences Cited [56] cell locations. Subsequently, the memory means will U.S. PATENT DOCUMENTS empond to any of these addresses and, through insera-345/173-80 1.414,754 4/1969 345/173 30 3,458,273 4/1972 3,348,853 7/1973 Murchall 3.748.853 7/1973 145/123-10 of the addressed faulty cell. 160/173 10 Requested. 1.800.294 3/18/14 Lawbr 340/173 10 5/1974 MD/173 DD



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### TMS 1000







## IBM 370/168 – circa 1974



"I think there is a world market for maybe five computers", Thomas J. Watson (1943)

# 1978 <mark>- 1</mark>995

THE

## **Digital Equipment Corporation**

17.5 Year Ody

http://research.microsoft.com/en-us/um/people/gbell/Digital/timeline/1978.htm

at



# 1977: VAX-11/780 – STAR is Born!





**Evolution of VAX Architecture:** 

VAX-11 Architecture

Reference Manual

**Floating Point Extensions** 

# 1985: MicroVAX-II (Subset ISA)





The MicroVAX-I (Seahorse), introduced in October 1984, was the first VAX computer to use VLSI Technology.



# 1988-1992: VAX 6000 Series



when you care enough to steal the very best

## 1989: VAX 9000 - The Age of Aquarius



### The Beginning of the End of VAX

## **RISC vs CISC WARS**

- Sun SPARC
- MIPS R2000, R3000, R4000, R6000, R10000
- PA-RISC
- IBM Power and Power PC
- DEC Alpha 21064, 21164, 21264

In 1987, the introduction of RISC processors based on Sun's SPARC architecture spawned the now famous RISC vs CISC debates. DEC cancelled PRISM in 1988. RISC processors from MIPS, IBM (Power, Power PC), and HP (PA-RISC) started to gain market share. This forced Digital to adopt MIPS processors in 1989, and later introduce Alpha AXP (Almost eXactly PRISM!) in 1992.

### High Performance Issue Oriented Architecture

D. Bhandarkar, D. Orbits, R. Witek, W. Cardoza, D. Cutlert

**Digital Equipment** Corporation

microPRISM





## **RISC vs CISC Debate**

- VAX was king of CISC
  - More than 300 instructions of variable length
  - Compact code size
  - Hard to decode quickly
  - Low Freq, Short Path Length, Complex Design
- Iron Law of Performance:
  - Speed = IPC \* freq /Path Length
- **RISC championed by SPARC and MIPS** 
  - Simpler instruction format but longer path length
  - Higher frequency (Brainiacs vs Speed Demons)
- RISC was "better" for in order designs
- Out of order microarchitectures leveled the playing field
- Semiconductor Technology and Volume Economics matter!
- PC Volumes and Pentium Pro design changed the industry

The difference between theory and practice is always greater in practice than it is in theory!

Performance from Architecture: Comparing a RISC and a CISC with Similar Hardware Organization

> Dioty Blandsrine Digital Economic Corp. 148 Main Direct (MLOS-2/01) Maynard, MA 01754

Douglas W. Clark\* Allem Computation Lab-Harrard University Carabridge, MA 00138

#### Abstract

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#### 1 Introduction

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#### RISC versus CISC: A Tale of Two Chips

#### Dileep Bhandarkar intel Corporation Santa Ciara, California, USA

#### Abstract

This paper company as agamative RINC and CINC implementation built with comparable includings The new clique are the Alpha" 21168 and the Island Pennant" Ivo position. The paper present performance comparisons for industry standard enchmalits and unit performance cranker statistics to compare various aspects of hold-designs.

#### Introduction

In 1993, Ibustatur and Clark poblished a super-comparing an manple implementation from the RDC and CESC arthractural actions (a MEPS" MODOO and a Digkal VAN \$7001 on one of the int \$P\$CS9 tenchnuts. The organizational similarity of elese machines provided an opportunity to reachine the partly architectural advantages of RISC. That paper deserved that the ensulting advantage in cycles per program ranged from slightly under a factor of 2 to almost a factor of 4, with a geometric marg of 2.7. This paper alterapts yet another comparison of a brading EDC and COC implementation, but using chips imped with comparable semiconductor inclusiony. The RDC chip chosen for this multy is the Digital Abla 20164 (Edmonitors95). The CDSC chip is the Intel Postices" Pro processor (ColumPil). The results should son be used to draw ownepting conclusions about RDC and CDC in general. They should be normal as a mapping in time. New that performance is also intermined by the system stations and compiler and

#### Chip Overview

Table 3 shows the sugar characteristics of the two chips. Both chips are implemented to ansast 11.5pr technology and the ide tate is comparable. The design symmeth is used of Hermit, but both represent state of the ort implementation that attained the highest performance for KDC and CDC architecture respectively at the time of their introduction.

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The 21344 is a qual inner superscalar divige that implements two levels of ciartes on chip, that done not implement out of order electrics. The Postarelt Propressure implements dynamic execution using alant of order, amendative examine region with righter resuming of integer, floating print and flags sutubles. Consequently, even though the dir size is comparable, the total management process in upday different for the two chirs. The segmenting design of the Pentium Per processor is much more logic intensive, and hugi transmost are less dense. The ca-otag, 56, KD 12, cache of the 21164 inflates in transieur cont. Even Hough the Alpha 21118 has an smallip 3.3 cache, must system air a 2 or 4 100 board lived mathetics achieves their performance goal

# 1991: ACE Initiative



- The Advanced Computing Environment (ACE) was defined by an industry consortium in the early 1990s to be the next generation commodity computing platform, the successor to personal computers based on Intel's 32-bit x86 instruction set architecture.
- The consortium was announced on the 9th of April 1991 by MIPS Computer Systems, Digital Equipment Corporation, Compaq, Microsoft, and the Santa Cruz Operation.
- At the time it was widely believed that RISC-based systems would maintain a price/performance advantage over the x86 systems.
- The environment standardized on the MIPS architecture and two operating systems: SCO UNIX with Open Desktop and what would become Windows NT (originally named OS/2 3.0).
- The Advanced RISC Computing (ARC) document was produced to define hardware and firmware specifications for the platform.
- When the initiative started, MIPS R3000 RISC based systems had substantial performance advantage over Intel 80486 and original 60 MHz Pentium chips .
- MIPS R4000 schedule and performance slipped and Intel updated the Pentium design to 90 MHz in the next semiconductor process generation and the MIPS performance advantage slipped away.

## Strategy without Execution is Doomed!

# **Alpha was Too Little Too Late!**

**Computing/Microprocessor Applications** 

Appha Implementations and Architecture Complete Reference and Guide Dileep P. Bhandarkar

### Alpha Implementations and Architecture Complete Reference and Guide Dileep P. Bhandarkar

Alpha Implementations and Architecture provides a comprehensive description of all major aspects of Alpha systems. The bank includes an averview of the history of RISC development in the computer industry and at Digital, the Alpha erchitecture, of the major processor chips, and system implementations. Alpha implementations and Architecture also covers RISC concepts and design styles, and provides an everview of other RISC architectures, and descriptions of the new SPARC, MIPS, PowerPG, and PA-RISC microprocessors introduced in 1935. Other issues lipcosted include operating system parting, compiler techniques, and bioary translation.

Practicing computer engineers and graduate students in computer architecture alks will find this reference book invaluable as it describes the tradeality and design philoscophy that led to the development of the Alpha architecture and its implementations.

Dr. Dileop P. Obandarkar wrote this book while he was a Sanior Consuling Engineer and Hardware Technical Director in the Alpha Systems Bosiness Group at Bigital Equipment Corporation in Maynard, Massachusetts, He was responsible for leading the technical direction and product strategy of Alpha Personal Systems, Alpha and YAX servers, and High Performance Computing. He was the architecture manager for MicroVAR, chief architect for YAX vector processing, and on architect of the PRISM RISC architecture on which Alpha is based. Dr. Blandarkar has a B. Tirch, degree in electrical engineering from the Indian technical of Technology, Bomboy, and an M.S. and Ph.B. In electrical engineering from Carsegie Mellen University, and holds 15 U.S. patients. He is a senior member of IEEE and the

auther of more than 30 technical publications an computer architectura, semiconductor technology, and performance analysis. He is currently Director of System Portormance Analysis and Architecture at Intel Corporation in Sente Giara, California.





EV-T141E-DD



## Looking at Intel from the Outside



## 1974: 8080 Microprocessor



- The 8080 became the brain of the first personal computer--the Altair, allegedly named for a destination of the Starship *Enterprise* from the Star *Trek* television show. Computer hobbyists could purchase a kit for the Altair for \$395.
- Within months, it sold tens of thousands, creating the first PC back orders in history
- 2 MHz
- 4500 transistors
- 6 µm

# <u>1978-79: 8086-8088</u> <u>Microprocessor</u>



- A pivotal sale to IBM's new personal computer division made the 8088 the brain of IBM's new hit product--the IBM PC.
- The 8088's success propelled Intel into the ranks of the Fortune 500, and Fortune magazine named the company one of the "Business Triumphs of the Seventies."
- 5 MHz
- 29,000 transistors
- 3 µm

# 1981: First IBM PC



### The IBM Personal Computer ("PC")

- PC-DOS Operating System
- Microsoft BASIC programming language, which was built-in and included with every PC.
- Typical system for home use with a memory of 64K bytes, a single diskette drive and its own display, was priced around \$3,000.
- An expanded system for business with color graphics, two diskette drives, and a printer cost about \$4,500.

"There is no reason anyone would want a computer in their home." Ken Olsen, president Digital Equipment Corp (1977)

## 1979: Motorola 68000



### The 68000 became the dominant CPU for Unix-based workstations from Sun and Apollo

It was also used for personal computers such as the Apple Lisa, Macintosh, Amiga, and Atari ST

# 1985: Intel386™ Microprocessor



- The Intel386<sup>™</sup> microprocessor featured 275,000 transistors--more than 100 times as many as the original 4004. It was a Intel's first 32-bit chip.
- The 80386 included a paging translation unit, which made it much easier to implement operating systems that used virtual memory.
- 16 MHz
- 1.5µm

## 1989: Intel486™ DX CPU Microprocessor



- The Intel486<sup>™</sup> processor was the first to offer a "large" 8KB unified instruction and data on-chip cache and an integrated floating-point unit.
- Due to the tight pipelining, sequences of simple instructions (such as ALU reg, reg and ALU reg, im) could sustain a single clock cycle throughput (one instruction completed every clock).
- 25 MHz
- 1.2 M transistors
- 1 µm

# 1993: Intel® Pentium® Processor



- The Intel Pentium® processor was the first superscalar x86 microarchitecture. It included dual integer pipelines, a faster floatingpoint unit, wider data bus, separate instruction and data caches
- Famous for the FDIV bug!
- 22 March 1993
- 66 MHz
- 3.1 M transistors
- 0.8 µm

### Start of the sub-micron era!

# 1995: Intel® Pentium® Pro Processor



- Intel® Pentium® Pro processor was designed to fuel 32-bit server and workstation applications. Each processor was packaged together with a second L2 cache memory chip on the back-side bus.
- 5.5 million transistors.
- 1 November 1995
- 200 MHz
- 0.35µm
- 1<sup>st</sup> x86 to implement out of order execution
- Front side bus with split transactions
- The P6 micro-architecture lasted 3 generations from the Pentium Pro to Pentium III
- The Pentium Pro processor slightly outperformed the fastest RISC microprocessors on integer benchmarks, but floating-point performance was significantly lower



**P6** 

## The RISC Killer!

# June 1995: Inside Intel If You Can't Beat Them Join Them!




### 1997-98: Intel® Pentium® II Processor



 The 7.5 million-transistor 0.35 µm Pentium II processor was introduced with 512 KB L2 cache in external chips on the CPU module clocked at half the CPU's 300 MHz frequency in a "Slot 1" SECC module.

Klamath

Deschutes

 1998: Intel Pentium II Xeon processors (0.25 µm Deschutes) were launched with a full-speed custom 512 KB, 1 MB, or 2 MB L2 cache using a larger Slot 2 to meet the performance requirements of mid-range and higher servers and workstations



#### Mendocino

# 1998: Intel® Celeron® Processor



- The Intel® Celeron® processors were designed for the sub \$1000 Value PC market segment.
- The first Celeron processor (Covington) in April 1998 was just a 266 MHz Pentium II without a L2 cache
- Mendocino: First x86 with integrated L2 cache -128 KB
- 19M transistors
- 300 MHz
- 0.25µm
- 24 August 1998



Intel's Response to Cyrix 6x86 (M1)

# **1999: AMD Athlon**



Won the Race to 1 GHz

Sledgehammer

### Oct 2009: AMD Hammers Intel with AMD64



5 Oct 2009, SAN JOSE, California--Advanced Micro Devices today is detailing a new 64-bit chip that will compete against Intel's Itanium processor. The chip will be an extension of the current Intel-compatible chip design, or so-called x86 architecture, said Fred Weber, vice president of engineering at AMD's computation products group, at a processor industry conference here today. Intel's next-generation design, Itanium, will be a wholly new architecture.

# 1999: Intel® Pentium® III Processor – 0.18µm



- 25 Oct 1999
- Integrated 256KB L2 cache
- 733 MHz
- 28 M transistors

 1st Intel microprocessor to hit 1 GHz on 8-Mar-2000, a few days after AMD Athlon!

#### Willamette

# 2000: Intel® Pentium® 4 Processor – 0.18µm



- The Intel® Pentium® 4 processor's initial speed was 1.5 GigaHertz.
- 20 Nov 2000
- 256K integrated L2 cache
- Double clocked "Fireball" inner core
- Deep 20 stage pipeline
- 100 MHz quad pumped bus
- 42 M transistors
- Hit 2 GHz on 27 Aug 2001
- ~55 Watts
- No Mobile Pentium 4!



### High Frequency, but Power was High too!

# 2001: Intel® Itanium<sup>™</sup> Processor



- The Itanium<sup>™</sup> processor is the first in a family of 64-bit products from Intel. Designed for high-end, enterprise-class servers and workstations, the processor was built from the ground up with an entirely new architecture based on Intel's Explicitly Parallel Instruction Computing (EPIC) design technology.
- Based on HP's VLIW project
- May 2001
- 800 MHz
- 25M transistors
- 0.18µm
- 4 MB External Level 3 Cache
- Intel's EPIC Blunder!

# IT AIN'T PENTIUM !!!



#### Northwood

# 2001: Intel® Pentium® 4 Processor – 0.13µm



- 27 August 2001
- 55 million transistors
- 2 GHz
- 512KB L2 cache
- In 2002 Intel released a Xeon branded CPU, codenamed "Prestonia" with Intel's Hyper-Threading Technology
- 14 Nov 2002: 3.06 GHz
- 23 June 2003: 3.2 GHz

Simultaneous Multi Threading Introduced to x86 Processors

# 2003: AMD Opteron – First 64 bit x86



First x86 processor with 64 bits and Integrated Memory Controller

# 2003: Intel® Pentium® M Processor



- The first Intel® Pentium® M processor, the Intel® 855 chipset family, and the Intel® PRO/Wireless 2100 network connection were the three components of Intel® Centrino™ mobile technology, with built-in wireless LAN capability and breakthrough mobile performance. It enabled extended battery life and thinner, lighter mobile computers.
- Was originally intended as part of Celeron family
- 12 March 2003
- 130 nm
- 1.6 GHz
- 77 million transistors
- 1 MB integrated L2 cache

The move away from core frequency to performance begins!

#### Prescott

# 2004: Intel® Pentium® 4 Processor – 90 nm



- 1MB L2 cache
- 64-bit extensions compatible with AMD64 (Humble Pie!)
- 120 million transistors
- 31 stage pipeline
- Execution Trace Cache
- 3+ GHz frequency
- ~90 Watts (Ouch!)

### Frequency Push Gone Crazy!

### 2005: First Dual Core Opteron



#### Beginning of the Multi-Core Era!

### 2005: Last Netburst Microarchitecture Core (65nm)

Cedar Mill



### Finally the Frequency Madness Ends!

# **Increasing Energy Efficiency**



# 2006: Intel's 1st Monolithic Dual Core



- January 2006
- Intel® Core<sup>™</sup> Duo Processor
- 90 mm<sup>2</sup>
- 151M transistors
- 65 nm
- First Intel processor to be used in Apple Macintosh Computers

The Convergence to Multiple Mobile Cores Begins Finally!

# Why Multi-Core Processor Chips?

- With Each Process Generation transistor density doubles
  - Frequency had increased by ~1.5X; ~1.3x in future
  - Vcc had scaled by about ~0.8x; ~0.9x in future
  - Capacitance had scaled by 0.7x; ~0.8 in future
  - Total power may not scale down due to increased leakage
- Instruction Level Parallelism harder to find
- Increasing single-stream performance often requires non-linear increase in design complexity, die size, and power
- Many server applications are inherently "parallel"
- Parallelism exists in multimedia applications
- Multi-tasking usage models becoming popular

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2007 Intel Distinguished Lecture

## Multi-Core Energy-Efficient Performance



# 2003\_2004\_2006

# July 27, 2006



### **2006: Intel<sup>®</sup> Core<sup>™</sup> Micro-architecture Products**

Intel<sup>®</sup> Wide **Dynamic** Execution Intel<sup>®</sup> Intelligent Power Capability Intel<sup>®</sup> Advanced **Smart Cache** Intel<sup>®</sup> Smart Memory Access Intel<sup>®</sup> Advanced **Digital Media** 

Boost





inte

WOODCREST

The Empire Strikes Back! Thanks to Israel Design Center!



### Moore's Law Enables Microprocessor Advances

Chatting with Gordon Moore http://www.youtube.com/watch?v=xzxpO0N5Amc

1.0µm 0.8µm 0.6µm 0.35µm 0.25µm 0.18µm 0.13µm 90nm 65nm

Intel 486™ Processor



Pentium<sup>®</sup> Processor







Pentium<sup>®</sup> II/III Processor





Source: Intel









Intel® Core<sup>™</sup> Duo Processor Intel® Core<sup>™</sup> 2 Duo Processor

New Designs serve High End first and waterfall to more mainstream segments as die size decreases in subsequent nodes



#### Clovertown

### October 2006: The World's First x86 Quad-Core Processor (2 die in a package)



"Quick & Dirty" Innovation to drive Fast Time to Market!

### 2006: Itanium 2: First Billion Transistor Dual Core Chip (90nm) 1MB L21 2 Way



**Multi-threading** 

#### 2x12MB L3 Caches





**1.72 Billion Transistors (**596 mm<sup>2</sup>)

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Montecito

# From 2300 to >1Billion Transistors In < 40 Years of Moore's Law

Moore's Law video at http://www.cs.ucr.edu/~gupta/hpca9/HPCA-PDFs/Moores\_Law\_Video\_HPCA9.wmv



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# 2007: Dual Core Penryn

Penryn



45 nm next generation Intel® Core<sup>™</sup>2 family processor 410 million transistors *World's first working 45 nm CPU Introduced Turbo Mode Production in the November 2007* My Last Hurrah at Intel: <u>http://blogs.intel.com/technology/2007/04/penryn/</u>

# 2007: Bill Gates Wants You!



### 2007: AMD Barcelona First Monolithic x86 Quad Core



#### How AMD turned Barcelona into a right royal mess

Analysis The problem, the protagonists, and where to go from here

#### By Charlie Demerjian Sat Dec 08 2007, 13:22

#### Chip problem limits supply of quad-core Opterons

by Scott Wasson - 1:49 PM on December 3, 2007

AMD's quad-core "Barcelona" Opterons have been notably difficult to find since their introduction two months ago, and The Tech Report has learned that a chip-level problem has impacted the supply of these chips to both server OEMs and distribution channel customers.

283mm<sup>2</sup> design with 463M transistors to implement four cores and a shared 2MB L3 cache in AMD's 65nm process

# 2008-9: Performance Race Gets Serious With Quad Core





AMD Barcelona

**Intel Nehalem** 

Intel finally integrates Memory Controller and abandons shared Front Side Bus









2010: Intel Westmere

### **Data Centers at Microsoft**



# **Cloud Optimized High Density Servers**







Servers built using commodity components (Low Power 2 socket CPUs, SATA HDD, MLC SSD) No redundancy features in hardware (e.g. RAID, dual Power Supplies) Applications specifically designed to provide Resiliency and Fault Tolerance

# **2013: Catching The Smartphone Wave!**



# **Disruptions Come from Below!**



## Era of Small Cores (circa 2013)

• Intel Atom (32 nm Clover Trail)











1.90 mm

### WIRED

#### The Data Centers of Tomorrow Will Use the Same Tech **Our Phones Do**

By Peter Levine | Monday August 4, 2014

Share 0 Tweet 620 8+1 0 Pinit 8

Today, the mobile phone industry is where so much innovation has been concentrated-resulting in an entirely new class of components created just for this smaller form factor: flash memory, smaller CPUs, networking hardware, and so on. Which means lightweight processors (such as ARM) and low-cost, lowpower mobile components are now becoming the foundation of the next-generation datacenter.

### MICROPROCESSOR <u>report</u>

#### Insightful Analysis of Processor Technology

#### BROADCOM BARES MUSCULAR ARM

Quad-Issue ARMv8 CPU Targets Xeon-Class Performance

By Linley Gwennap (October 21, 2013)

### MICROPROCESSOR <u>report</u>

Insightful Analysis of Processor Technology

#### THUNDERX RATTLES SERVER MARKET

Cavium Develops 48-Core ARM Processor to Challenge Xeon

By Linley Gwennap (June 9, 2014)

CAVIUM

Applied Micro's X-Gene challenges for server processor market

📰 to commany 🚊 dataf manager 📀 (bh. August 2014) 🔟 Germany by small

Applied Micro leads the charge to infiltrate the \$12 billion server processor market with ARM-based ICs.

This is not a trivial task. The \$54 billion gonlia standing in Applied Micro's way is intel with a 90% plus share of the server processor market

So what, if any, are Applied Micro's selling points compared to intells?

First and foremost there's the business model

"Competition is what we're bringing," says Gauray Singh, vp of technical strategy at Applied Micro. 'in must other markets there is very healthy competition with multiple alicon customera."

#### Weekly.com

BROADCOM



#### Intel juices up microserver speeds with thrifty Avoton chip



Summary: Intel is claiming to have made significant strides in performance and power efficiency in the microserver market with its new Avoton system on a chip.

Barcelona Supercomputing Center

Centro Nacional de Supercomputación

**EUROPE WANTS** 

**A SMARTPHONE** 

SUPERCOMPUTER

A consortium hopes to build exaflop

supercomputers from mobile CPUs

#### ZDNet

#### AMD Announces the Availability of 64-bit ARM Opteron Developer Kits

#### JUDAWALE CARE 7/36/2014

#### esture: AMD's first of bit details and processic, codevaned "leattle" AMD is the first consuley to provide a standard ARM Contex#457, based server eletterer for arthrown developers and integration. Software and herdware developers as well as early adopters to large datacenters are explore and can apply on AMD's ambiti

The pairney toward a more efficient infractuature for large-scale datacenters is taking a region stap Torward today with eter availability of our 4MD Opterion A1100 Series development bit," paid furnish Gooplaintshwan, general manager and ics precident, Server Euphress unit, AMD. "When successfully sensiting to regist ecosystem partners such as Fretraines, OS, and tools providers, we are taking the next stap in what will be a collaborative effort across the industry to reimagine the dataparter hand on the open in sinear result of all his incomption

With this encouncement, AMD becomes the only provider of 64-bit ARM server hardware with complete ARM/d instruct suggest to foster the development of the ecosystem for efficient storage. Web applications and hosting, AMD is the only provider to offer the standard ARM Cartas AS7 technology

Contact:

IN AND FRAMEWORK STATISTICS.

Reisten Lika AMD Public Relations (902) 602-6633

### The Smart Phone Era Is Redefining Computing



"The phone in your pocket will be as much of a computer as anyone needs". – Dr. Irwin Jacobs, 2000

### **PC Market Shift**

2013 2014 2015



Source: www.pctoday.com
## **Continued Smartphone Momentum**

~20% CAGR for smartphone unit shipments expected between 2012-2017



Cumulative smartphone unit shipments forecast between 2013-2017



## Smartphone System Architecture



Snapdragon 800

Technology Cycles – Still Early Cycle on Smartphones + Tablets, Now Wearables Coming on Strong, Faster than Typical 10-Year Cycle



Image Source: Computersciencelab.com, Wikipedia, IBM, Apple, Google, NTT docomo, Google, Jawbone, Pebble.

## Learn to Wear Many Hats!



"Don't be encumbered by past history, go off and do something wonderful." - Bob Noyce, Intel Founder

## Questions?