OPEN
Compute Project

AMD Motherboard Hardware v1.0

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1 Scope

This document defines the technical specifications for the AMD motherboard used in Open Compute Project servers.

2 Contents

3   Overview

When data center design and hardware design move in concert, they can improve efficiency and reduce power consumption. To this end, the Open Compute Project is a set of technologies that reduces energy consumption and cost, increases reliability and choice in the marketplace, and simplifies operations and maintenance. One key objective is openness—the project is starting with the opening of the specifications and mechanical designs for the major components of a data center, and the efficiency results achieved at facilities using Open Compute technologies.

One component of this project is a custom motherboard. This document describes the Open Compute Project AMD motherboard, a dual AMD G34 socket motherboard with 24 DIMM slots. The motherboard is power-optimized and barebones, designed to provide the lowest capital and operating costs. Many features found in traditional motherboards have been removed from the design.

3.1   License

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4   Motherboard Features

4.1   Block Diagram

Figure 1 illustrates the functional block diagram of the motherboard.
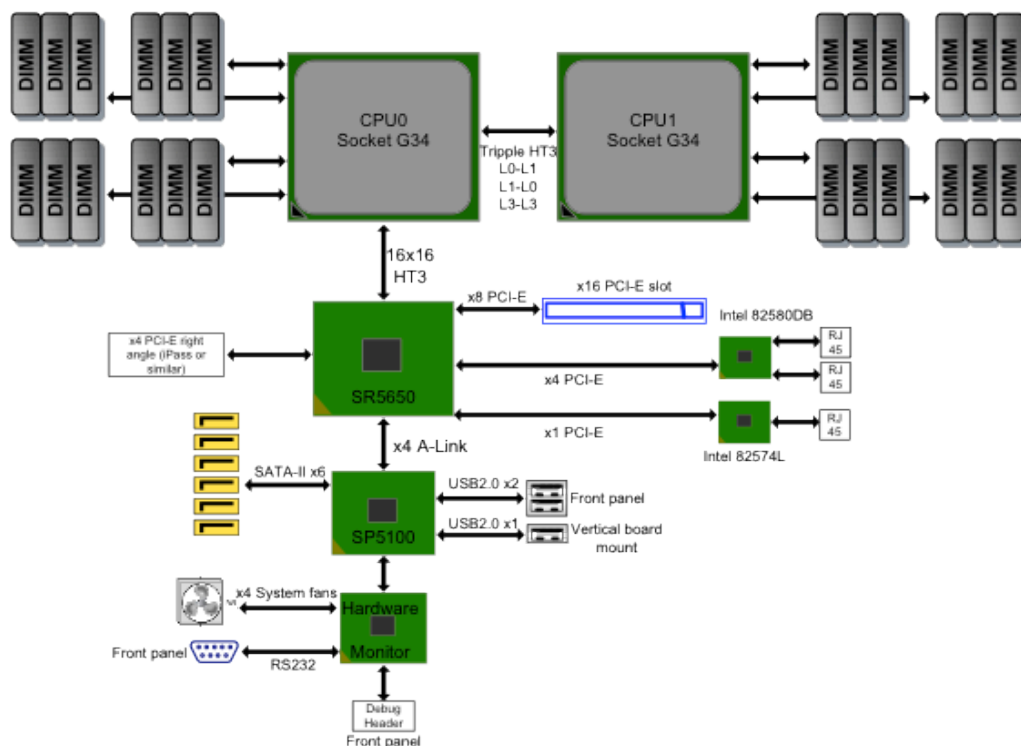
Figure 1 Functional Block Diagram

4.2   CPU and Memory

The motherboard uses AMD's Magny-Cours 12 and 8 core CPUs with a TDP (thermal design power) of 85W. The motherboard supports these features:

- HT3 16x16 link HyperTransport™ links between CPUs with cHT3 target of up to 6.4 GT/s
- 1 ncHT3 16x16 link to SR5650 chipset with target speed of up to 5.2 GT/s
- G34 socket infrastructure
- Power delivery per CPU for Infrastructure group-C (85W TDP)
- Single Processor Mode
- RDDR3 direct attached memory support on cpu0 and cpu1 with:
  - 4 channels DDR3 registered memory interface on processors 0 and 1
  - 3 DDR3 slots per channel per processor (total of 24 DIMMs on the motherboard)
  - 1.25V and 1.35V DDR3 memory
  - Up to maximum 384 GB memory with dual-rank 16GB RDIMMs
- Address Parity Enabled DIMMs
- 1R, 2R, and 4R RDIMMs and LRDIMM on 3 DIMMs per channel
- The following memory speeds must be supported:
  - Up to 1333 MT/s on 2 DIMMs/channel
  - Up to 1066 MT/s on 3 DIMMs/channel

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4.3   Northbridge

The design employs the AMD SR5650 chipset. The SR5650 has 22 PCI-E Gen lanes and 16x16 HyperTransport lanes. The 16x16 HyperTransport lanes are used for interconnect to P0 and the PCI-E lanes are distributed according to Figure 2.

Device	Number of PCI-E Lanes
Intel 82580DB NIC	4
Intel 82574 NIC	1
x16 Vertical Connector	8
X4 Right Angle Connector	4
Total number of lanes	17

Figure 2 PCI-E Lane Usage

4.4   Southbridge/Peripheral Bus Controller

The motherboard uses the AMD SP5100 Southbridge chipset. The SP5100 supports the following features:
- PCI bridge
- 3 USB 2.0 ports (two to front panel, one vertical onboard)
- 6 SATAII ports
- SPI interface (SPI part with density up to 4 MB)
- SMBUS interface (master and slave)
- UARTs interface routed to front panel

4.5   Network Interfaces

The motherboard has two options for network interfaces. Footprints, for the network chips, their respective RJ45 connectors and the PCI-E lanes are placed on the circuit board. The BIOS supports both of these network chips:
- Intel 82580DB dual Gigabit Ethernet chipset: Both Gigabit Ethernet interfaces are on the front panel. The 82580DB interfaces the SR5650 via x4 PCI-E lanes.
- Intel 82574L Gigabit Ethernet chipset: A single Ethernet interface is on the front panel RJ45 connectors. A single PCI-E lane is routed from the SR5650 to the 82574L network chip.

4.6   I2C Bus

The ODM must supply detailed I2C bus maps. The maps should include bus masters, muxes, and slaves. The ODM provides addresses for all devices on the I2C bus.

5 Power System

5.1 Input Voltage

5.1.1 Input Voltage Level

The nominal input voltage delivered by the power supply is 12.5VDC. The motherboard can accept and operate normally at the nominal input ±5%.

5.1.2 Capacitive Load

To ensure compatibility with the system power supply, the motherboard may not have a capacitive load greater than 8000μF. The capacitive load of the motherboard should not exceed the maximum value of 8000μF under any operating condition listed in section Figure 13, which defines environmental conditions.

5.1.3 Input Connector

The power input connector is an FCI 51733-009LF right-angle press-fit header. Details on the input power connector are in section 10.1.

5.2 CPU Voltage Regulation Module (VRM)

5.2.1 CPU Maximum Power

The motherboard can handle a processor with a maximum thermal design power (TDP) of 85W.

5.2.2 CPU VRM Optimizations

CPU VRM is optimized to reduce cost and increase the efficiency of the power conversion system. The ODM should only use the minimum number of required phases to support the maximum CPU power defined in 5.2.1. A PSI (power state indicator) allows the shedding of unused phases, letting the VRM operate at its peak efficiency.

5.2.3 CPU VRM Efficiency

The minimum efficiency for the CPU VRM is 91% over the 30% to 90% load range, measured from the 12.5V input to the VRM output.

5.3 Hard Drive Power

The motherboard supplies power to the system's six hard drives. The drives require 12VDC and 5VDC power sources. Power is delivered through a traditional 4 pin floppy disk power connector described in section 10.2.

5.3.1 Power Requirements

In order for the motherboard to supply 12.5VDC power to the hard drives, the PCB traces can support 1A of continuous power per drive and the inrush current required to start the drive from idle. In order for the system's 5VDC to supply power to all six hard drives, its regulator must support an additional 4.5A (0.750A per drive) continuous and must support the inrush current required by each drive.

5.3.2 Output Protection

The 5V disk output power regulator protects against shorts and overload conditions.

5.3.3 Spin-up Delay

When the hard drive spins up after the system powers on, it draws excessive current on both 12V and 5V. The peak current may reach 1.5A - 2A range in 12V. The system can have up to six hard drives installed, so the hard drives must spin up in sequence. The BIOS implements a 5 second delay between each hard drive spinning up.

5.4 System VRM Efficiency

The ODM must supply high efficiency VRMs for all other voltage regulators over 20W not defined in this specification. All voltage regulation modules over 20W have 91% efficiency over the 30% to 90% load range.

5.5 Power On

The motherboard powers on upon application of power to the input connector. The use of a power button is not required. The motherboard always resumes operation upon restoration of power in a power failure event.

6 BIOS

The ODM is responsible for supplying and customizing a BIOS for the motherboard. The specific BIOS requirements are outlined in this section.

6.1 BIOS Interface and Size

The BIOS interfaces the SP5100 via the SPI bus. The ODM is responsible for selecting a specific BIOS chip that meets the required functionality.

6.2 BIOS Socket

A socket must be used to mount the BIOS chip onto the motherboard. To ensure that the BIOS can be replaced manually, the BIOS chip is not soldered to the motherboard. The BIOS socket is easily accessible; other components on the motherboard do not interfere with the insertion or removal of the BIOS chip.

6.3 BIOS Configuration and Features

The BIOS is tuned to minimize system power consumption. It has the following features:
- C1E power state
- Unused PCI-E lanes disabled
- Unused PCI lanes disabled
- Option to disable the x8 (x16 physical) PCI-E slot
- Unused USB ports disabled

In addition to the power saving features, the BIOS also supports these features:
- USB keyboards
- Restore to the "ON" state after power loss
- Display power on self test (POST) results during boot up

6.4   BIOS Menu

The BIOS has a boot menu that allows options to be configured before the operating system loads. The BIOS supports USB keyboards for navigating the BIOS menu. The configuration options available through the boot menu include the following:

- Boot device selection
- Boot device priority
- Enable/disable watchdog timer (see section 9.4)
- Restore default settings
- Hardware monitor values (see section 9)
- Enable/disable extended memory test (quick boot)

6.5   Console Redirect

The BIOS detects the presence of a video card in the x16 PCI-E slot. If a video card is present, the BIOS directs its output to the video card. If no video card is present, the BIOS directs its output to the board-mounted RS-232 console output.

6.6   PXE Boot

The BIOS supports Intel PXE boot. When PXE booting, the system first attempts to PXE boot from the first Ethernet interface (eth0). If a PXE boot on the first Ethernet interface fails, the BIOS attempts to PXE boot from the second Ethernet interface (eth1).

6.7   Remote BIOS Update

The BIOS can be updated remotely under these scenarios:

- Scenario 1: Sample/Audit BIOS settings

  o Return current BIOS settings, or
  o Save/export BIOS settings in a human-readable form that can be restored/imported (as in scenario 2)

- Scenario 2: Update BIOS with pre-configured set of BIOS settings

  o Update/change multiple BIOS settings
  o Reboot

- Scenario 3: BIOS/firmware update with a new revision

  o Load new BIOS/firmware on machine and update, retaining current BIOS settings
  o Reboot

Additionally, the update tool(s) should have the following capabilities:

- Update from the operating system over the LAN – the OS standard is CentOS v5.2
- Can complete update with a single reboot (no PXE boot, no multiple reboots)
- Minimal user interaction (like prompts)
- Can be scripted and propagated to multiple machines

6.8   Event Log

Per the SMBIOS specification Rev 2.6, the BIOS implements SMBIOS type 15 for an event log; the assigned area is large enough to hold more than 500 event records (assuming the maximum event record length is 24 bytes, then the size will be larger than 12KB), and

follow the SMBIOS event log organization format for the event log. The ODM must provide a system access interface and application software to retrieve and clear the event log from the BIOS, including, at minimum, a Linux application for the CentOS operating system and driver as needed. The event log must be retrieved and stored as a readable text file that is easy to handle by a scripting language under Linux.

6.8.1   Logged Errors

- **CPU/memory errors**: Both correctable ECC and uncorrectable ECC errors should be logged into event log. Error categories include DRAM, Link, and L3 Cache.
- **HT errors**: Any errors that have a status register should be logged into the event log. Fatal or non-fatal classification follows the chipset vendor's recommendation.
- **Internal parity errors**: All errors which have status register should be logged into Event Log. Fatal, non-fatal, or correctable classification follows the chipset vendor's recommendation.
- **PCIe errors**: All errors which have status register should be logged into Event Log, including root complex, endpoint device and any switch upstream/downstream ports if available. Link disable on errors should also be logged. Fatal, non-fatal, or correctable classification follows the chipset vendor's recommendation.
- **POST errors**: All POST errors detected by the BIOS during POST should be logged into the event log.

6.8.2   Error Threshold Setting

Enable error threshold setting for both correctable and uncorrectable errors, once programmed threshold is reached, an event should be trigged and logged.

- **Memory Correctable ECC**: The threshold value is 1000. When the threshold is reached, the BIOS should log the event including DIMM location information and output DIMM location code through the Facebook debug card.
- **HT errors**: Follow the chipset vendor's suggestion.
- **PCIE errors**: Follow the chipset vendor's suggestion.

7   Reboot on LAN

Reboot on LAN (ROL) is a feature that repurposes the traditional Wake on LAN (WOL) signal to reboot the motherboard. When a WOL packet is received by the NIC, the interrupt generated by the NIC causes a hardware reboot of the motherboard. This is accomplished by tying the WOL interrupt pin of the NIC to the system's master reboot signal. ROL does not require the power supply to cycle its output. There is an optional ROL connection for the WAKE# signal from PCI-E slot and external PCI-E connector, which gives optional ROL support for add-in cards and external PCI-E devices. If the motherboard is in a low power state, the ROL signal causes the motherboard to exit the low power state.

8   Debug Header

The motherboard includes a debug header to display POST codes. The POST codes are sent to a board-mounted header in hexadecimal format via two 4-bit hex codes. The hex codes can be driven by either the legacy parallel port (port 80) on the hardware monitor, or 8 GPIO pins. A debug card with two 7-segment displays, two hex-to-7 segment

converters, logic level to RS-232 shifter, and an RS-232 connector interfaces the debug header.

8.1   POST Codes

During the boot sequence, the BIOS initializes and tests each DIMM. If a module fails initialization or does not pass the BIOS test, one of the following POST codes will flash on the debug card to identify the problematic DIMM. The first hex character indicates which CPU interfaces the DIMM; the second hex character indicates the number of the DIMM. The BIOS flashes the corresponding hex code indefinitely to allow time for a technician to service the system. The DIMM number count starts from the DIMM furthest from the CPU.

Code	Result	Code	Result
A0	CPU 0 DIMM 0 Failure	B0	CPU 1 DIMM 0 Failure
A1	CPU 0 DIMM 1 Failure	B1	CPU 1 DIMM 1 Failure
A2	CPU 0 DIMM 2 Failure	B2	CPU 1 DIMM 2 Failure
A3	CPU 0 DIMM 3 Failure	B3	CPU 1 DIMM 3 Failure
A4	CPU 0 DIMM 4 Failure	B4	CPU 1 DIMM 4 Failure
A5	CPU 0 DIMM 5 Failure	B5	CPU 1 DIMM 5 Failure
A6	CPU 0 DIMM 6 Failure	B6	CPU 1 DIMM 6 Failure
A7	CPU 0 DIMM 7 Failure	B7	CPU 1 DIMM 7 Failure
A8	CPU 0 DIMM 8 Failure	B8	CPU 1 DIMM 8 Failure
A9	CPU 0 DIMM 9 Failure	B9	CPU 1 DIMM 9 Failure
AA	CPU 0 DIMM 10 Failure	BA	CPU 1 DIMM 10 Failure
AB	CPU 0 DIMM 11 Failure	BB	CPU 1 DIMM 11 Failure

Figure 3 BIOS POST Codes

8.2   Serial Console

The output stage of the system's serial console is contained on the debug card. The TX and RX signals from the hardware monitor chip are sent to the debug header at the chip's logic levels (+3.3V). The debug card contains the RS-232 level shifter and the RS-232 D-9 connector.

8.3   System Reset

The master reset signal is routed to the debug header. If the master reset signal is connected to ground, the motherboard performs a complete system reset.

8.4   Debug Connector

The connector for the debug header is a 14-pin, shrouded, vertical, Molex C-Grid connector. The connector is mounted on the front connector side of the PCB. See section 10.4.3 for details on the positioning and pin out.

8.5 Bring-up Headers

The motherboard includes an HDT+/SCAN header and a Vref margin header for bring-up. The exact location of these headers may be determined by the ODM, but they cannot interfere with other components on the motherboard.

9 Hardware Monitoring

The motherboard does not employ a traditional out of band monitoring solution. A desktop style hardware monitor chip is used to collect temperatures, drive fans, and create a watchdog hardware monitor. The ODM should propose a hardware monitor chip that meets the requirements defined in this section. The ODM needs to provide a system access interface and application to retrieve hardware monitoring sensor readings, including at minimum, a Linux application for the CentOS operating system and driver if needed. The sensors to be read include voltage, temperature, and fan speed.

9.1 Temperature Sensors

The hardware monitor interfaces with each CPU's side band temperature sensor interface (SB-TSI) and the board-mounted thermal sensors. There is one sensor in the front of the motherboard to measure inlet air temperature, and another in the rear of the motherboard to measure outlet temperature. The ODM is responsible for determining the offset and calibration registers for all thermal sensors.

9.2 Fan Control and Feedback

The hardware monitor controls the four system fan speeds using a 25kHz fan PWM signal. Each of the four fans may be driven by the same PWM signal. The tachometer feedback signal from each of the four fans must be acquired by the hardware monitor. Both control and feedback signals must comply with the requirements defined in the *4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification* Revision 1.2 July 2004 published by Intel Corporation.

9.3 Fan Control Algorithm

The ODM must provide a fan control algorithm that ensures adequate cooling of the system in the chassis. The fan control algorithm optimizes the usage of fan power and the power consumed by leakage in the components. Under no operating conditions should any component exceed its maximum operating temperature.

9.4 Watchdog Timer

The hardware monitor employs a watchdog timer that reboots the motherboard if it is not cleared before the timer expires. The timer is adjustable and has a default timeout of 15 minutes. The time can be adjustable in one-minute increments from 1 to 30 minutes. The timer can be enabled and disabled using the BIOS menu. The default BIOS configuration has the timer enabled.

10 Connectors and Headers

10.1 Input Power Connector

The power input connector is an FCI 51733-009LF right-angle press-fit header. The connector has two positive terminals and two negative terminals with a blank (empty) slot between the pairs of contacts. The mating connector on the system power supply is an FCI 51773-005LF. Positioning of the connector on the motherboard is defined in section 11.4.

Power is distributed to the CPUs across pin 1 of the power connector. The rest of the system is powered through pin 2. Figure 4 illustrates the input power connector pin usage.

pin 4–GND
pin 3–GND

pin 2–system power
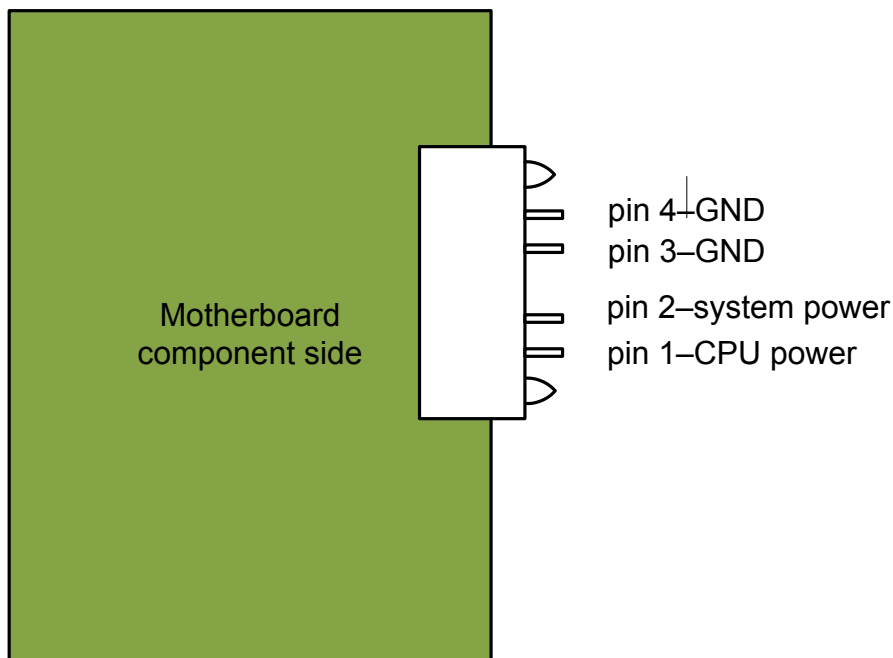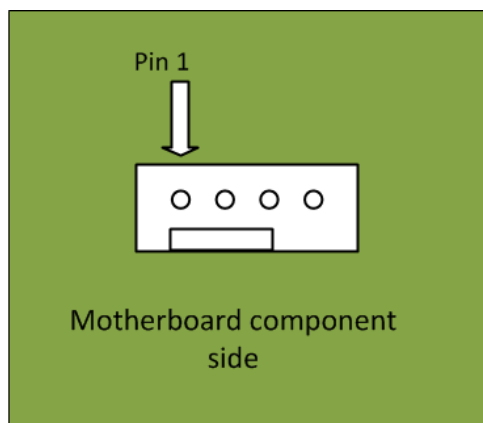pin 1–CPU power

Motherboard component side

Figure 4 Input Power Distribution

10.2 Drive Power Connector

The motherboard supplies power to six hard drives via a traditional 4-pin floppy disk power connector. The pin assignment follows the industry standard convention described in Figure 5.

Pin	Description
1	+5VDC
2	GND
3	GND
4	+12VDC

Figure 5 Drive Power Connector

10.3 External PCI Express

Four PCI-E lanes from the Northbridge are routed to a front-panel off-board right-angle connector. The on-board connector is a miniSAS-4i type right-angle connector, Molex 75783-0140. Figure 6 shows the required external PCI-E pin assignments. The design follows the *PCI Express External Cabling Specification* Rev1.0.

Pin Numbers	Signals	Description
A2/A3, A5/A6, A13/A14, A16/A17	PER{0..3}{P/N}	Differential PCI Express Receiver Lanes
A1, A4, A7, A12, A15, A18	GND	Ground Reference for Differential PCI Express Lanes
A8	CPRSNT#	Cable Installed/Downstream Subsystem Powered-up
A9	CPWRON	Upstream Subsystem's Power Valid Notification
A10	CWAKE#	Power Management Signal for Wakeup Events (Optional)
A11	CPERST#	Cable PERST#
B2/B3, B5/B6, B13/B14, B16/B17	PET{0..3}{P/N}	Differential PCI Express Transmitter Lanes
B1, B4, B7, B10, B12, B15, B18	GND	Ground Reference for Differential PCI Express Lanes
B8/B9	CREFCLK	Differential 100 MHz Cable Reference Clock
B11	SB_RTN	Signal Return for Single-Ended Sideband Signals

Figure 6 External PCI-E Pin Assignments

10.4 Front Panel

10.4.1 Switches

The front edge of the PCB has right angle pushbutton switches. One switch is used as the system's power button the second switch is used at the system's reset button.

If the power switch is depressed for less than four seconds, a Power Management Event is issued, indicating that the power switch has been triggered. If the power switch is depressed for more than four seconds, the motherboard performs a hard power off.

If the reset switch is depressed for any length of time, the motherboard performs a hard reset and begins executing the BIOS initialization code.

The functionality of each switch is indicated by a label on the motherboard's silkscreen. The location of the switches on the motherboard is illustrated in Figure 10.

10.4.2 LEDs

The motherboard has 3 LEDs on the front edge. Figure 7 below indicates the color and function of each LED as well as their silkscreen labels. The silkscreen indicates the functionality of each LED.

LED Color	Function	Silkscreen Label
Blue	Power LED. This LED has the same functionality of a traditional PC power LED. It illuminates only if the motherboard is in the power on state.	PWR
Green	Hard drive activity. This LED illuminates when there is activity on the motherboard's SATA hard drive interfaces.	HDD
Yellow	This LED replaces the functionality of the PC speaker. The motherboard causes the LED to light to illuminate for the same duration and sequence as the PC speaker would normally beep. The LED allows easier diagnosis in a noisy data center environment.	BEEP

Figure 7 LED Functionality

10.4.3 Post Header

The connector for the debug header is a 14-pin, shrouded, vertical, Molex C-Grid connector part number 0702461404. Figure 8 describes the configuration of the headers. The notch in the shroud faces the front panel of the motherboard.

Pin (CKT)	Function
1	Low HEX Character [0] least significant bit
2	Low HEX Character [1]
3	Low HEX Character [2]
4	Low HEX Character [3] most significant bit
5	High HEX Character [0] least significant bit
6	High HEX Character [1]
7	High HEX Character [2]
8	High HEX Character [3] most significant bit

9	Serial Transmit (motherboard transmit)
10	Serial Receive (motherboard receive)
11	System Reset
12	NC
13	GND
14	VCC (+5VDC)

Figure 8 Debug Header

10.5 PCI-E

The motherboard has a single PCI-E expansion slot. The slot has a single x16 mechanical form factor connector and, electrically, is populated only with x8 PCI-E lanes. The connector complies with the requirements defined in the *PCIe® Base 2.1 Specification* published by the PCI-SIG (Peripheral Component Interconnect Special Interest Group).

10.6 SATA

The motherboard has six SATA disk connectors. The location of these connectors is illustrated in Figure 10. The connector meets the mechanical and electrical properties defined by the Serial AZA International Organization in the specification entitled *Serial ATA Revision 3.0 Specification* (released June 2009).

10.7 Network/USB Interfaces

The motherboard has two RJ45 Ethernet connectors located on the front edge of the board. The location on the connectors is illustrated in Figure 10. Each RJ45 connector has two built-in LEDs. Facing the RJ45 connector, the left LED is single color green. When it is solidly illuminated, the link is active; blinking indicates activity. The right LED is dual color green/yellow, where green means 100M link speed while yellow means 1000M link speed.

The RJ45 connector labeled eth0 in Figure 10 has two USB ports. The RJ45 connector labeled eth1 in Figure 10 does not require any USB connectors.

10.8 Fan

The motherboard has 4 fan connectors. The location of the fan connectors is illustrated in Figure 10. The connectors comply both mechanically and electrically with the specifications defined in the *4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification* Revision 1.2 July 2004 published by Intel Corporation. Figure 9 defines the proper pin out of the connector.

Pin	Description
1	GND
2	12VDC
3	Sense
4	Control

Figure 9 Fan Header Pin-out

11 Mechanical

11.1 Dimensions

The motherboard dimensions are 13x13 inches. Facebook uses a common chassis to support several types of motherboards. As a result, the placement of certain components and mounting holes is critical and must be done according to this specification.

11.2 Component Placement

Figure 10 shows the motherboard component placement. Placement for the input power connector and the PCI-E x16 slot must be placed in the exact location detailed by this specification. For all other components ODMs are encouraged to place components close to the relative locations illustrated in the figure.
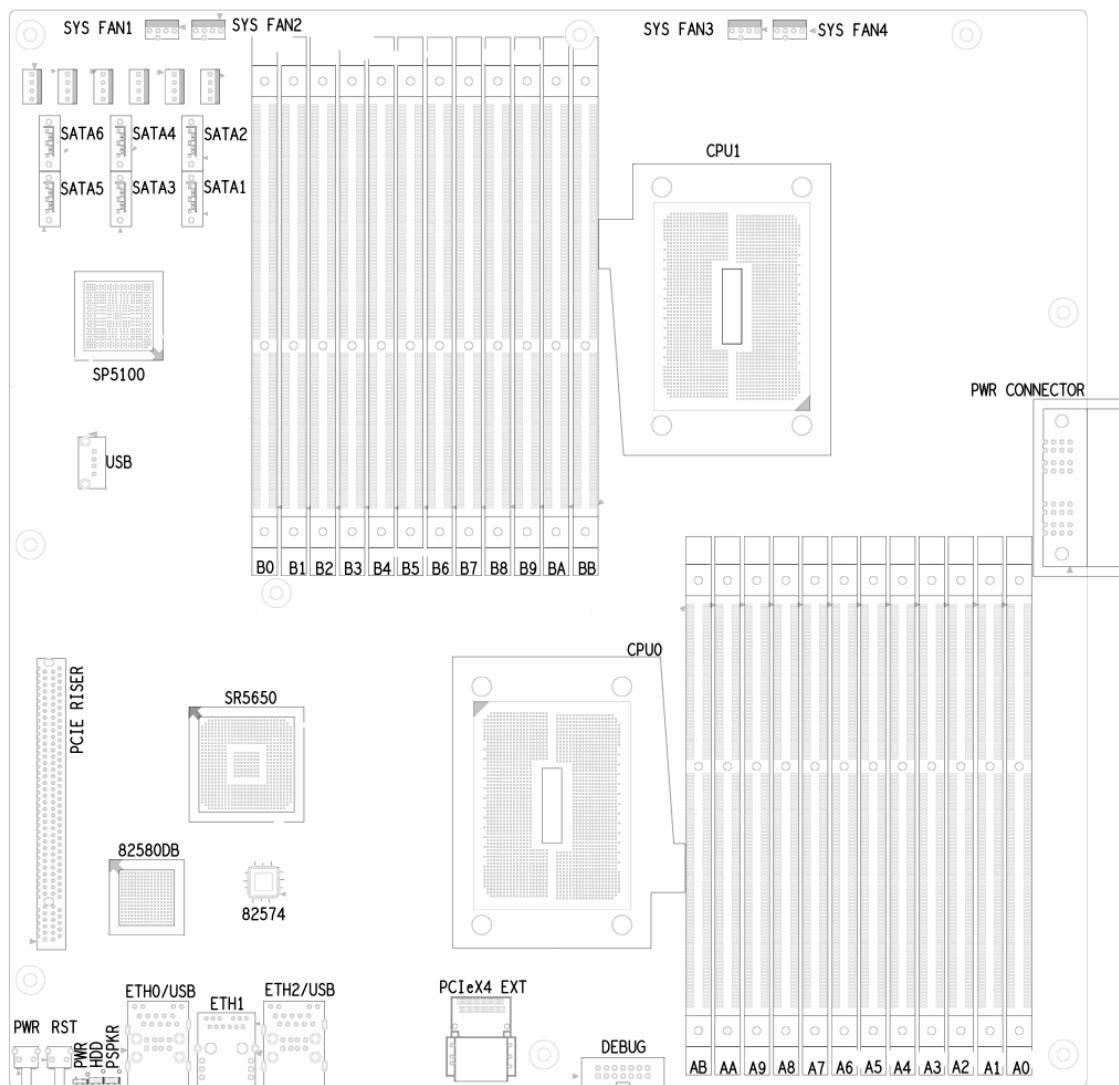

Figure 10 Recomended Component Placement

11.3   PCB Thickness

To ensure proper alignment of the FCI power connector and mounting within the mechanical enclosure, the PCB thickness is 2.2mm.

11.4   Input Power Connector

The input power connector is an FCI 51733-009LF right-angle press-fit header. The bottom of the FCI connector is pressed into the motherboard such that it is 2.37mm from the bottom of the motherboard. The exact position of the connector on the board is detailed in Figure 11 below. There is no need for a unique notch or cutout in the motherboard to support the connector. Detailed drawings can be found in section 14.
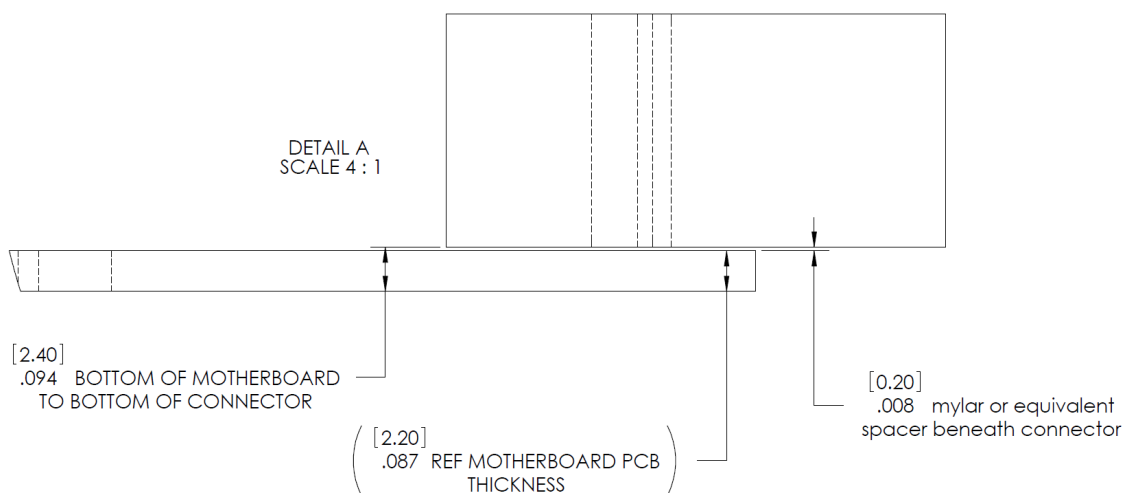
DETAIL A
SCALE 4 : 1

[2.40]
.094 BOTTOM OF MOTHERBOARD
TO BOTTOM OF CONNECTOR

[2.20]
.087 REF MOTHERBOARD PCB
THICKNESS

[0.20]
.008 mylar or equivalent
spacer beneath connector

Figure 11 Motherboard to FCI Connector Detail

Refer to the mechanical DXF file for detailed location of the power connector.

11.5   PCI-E Connector

The motherboard has one PCI-E x16 connector. The mechanical location of the connector will be in mounted according to the drawing below.

Refer to the mechanical DXF file for detailed location of the PCI-E connector.

11.6   Mounting Holes

Mounting holes must be located according to the mechanical DXF file for detailed location of the mounting holes.

11.7   Heat Sinks

The motherboard supports heat sinks that are mounted according to the 1U-2P heat sink assembly guidelines supplied by AMD in *Thermal Design Guide for the Socket G34 Processor Publication #45939* Rev: 1.00 November 2008. The ODM must comply with all keep out zones defined by AMD in the above specification.
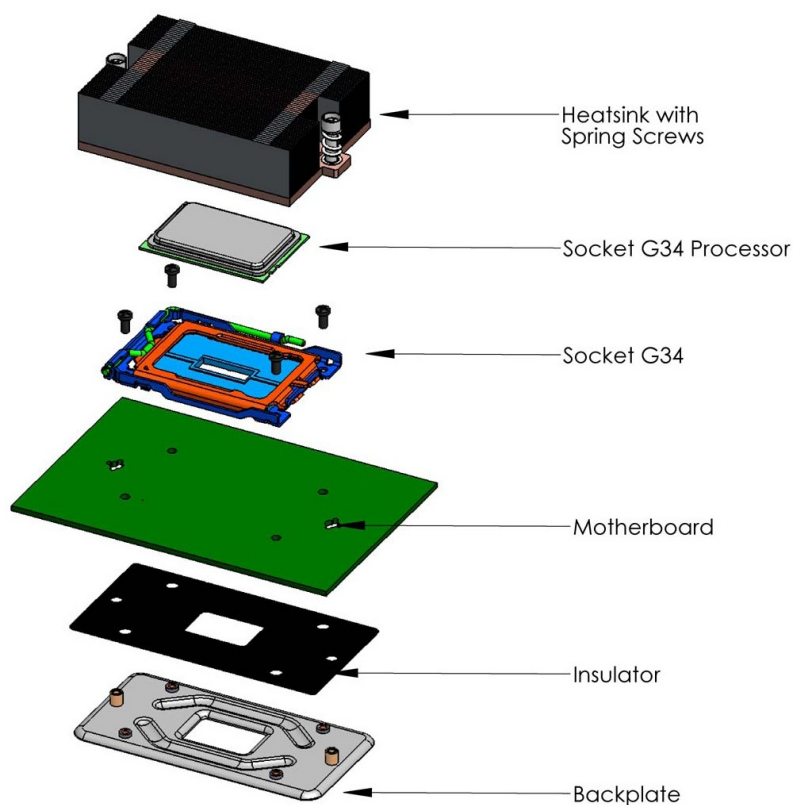
Figure 12 Heat Sink Mounting

11.8 Silkscreen

The silkscreen is white in color and includes labels for these components:
- cpu0/cpu1
- eth0/eth1
- DIMM slot numbering, 0-B for each CPU
- LEDs, as defined in 10.4.2
- Switches, as defined in 10.4.1

11.9 DIMM Connector Color

Colored DIMM connectors indicate the first DIMM of each memory channel, whereas the remaining DIMM connectors on the same memory channel are a different color. The first DIMM on each channel is defined as the DIMM placed physically furthest from its associated CPU. This DIMM connector must be populated first when memory is only partially populated.

11.10 Airflow

The motherboard is cooled using fans driven according to the CPU temperatures and the temperature reported by the motherboard mounted thermistor. See the *Open Compute Project Server Chassis and Triplet Hardware v1.0* specification for more details on the thermal operating conditions. Figure 13 illustrates the direction of airflow across the motherboard.

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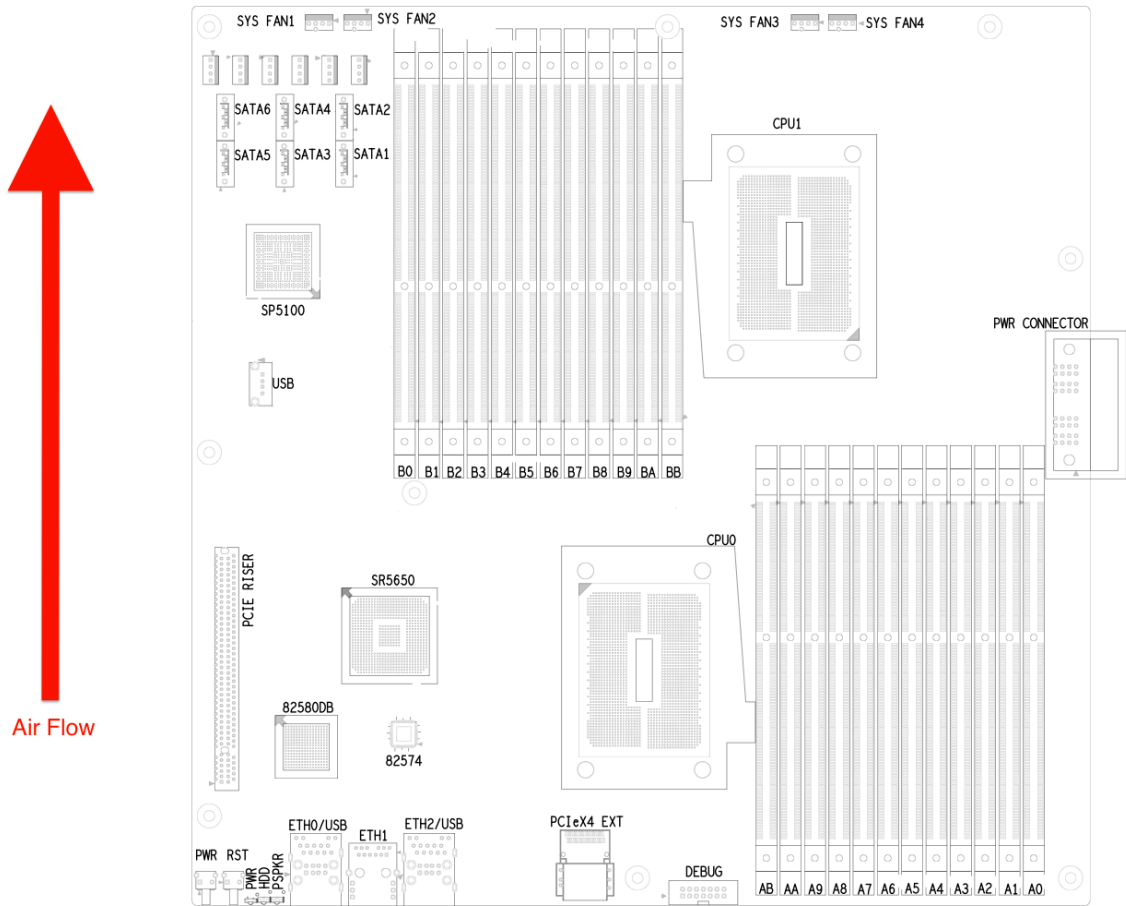
Figure 13 Airflow Direction

12 Environmental Requirements

The motherboard meets the following environmental requirements:
- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: -5°C to +45°C
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°C
- Transportation temperature range: -55°C to +85°C (short-term storage)
- Operating altitude with no de-ratings: 3000m (10000 feet)

12.1 Vibration and Shock

The motherboard meets shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard & Levels. The testing requirements are listed in Figure 14.

	Operating	Non-Operating
Vibration	0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)	1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute for each of the three axes (one sweep is 5 to 500 to 5 Hz)
Shock	6g, half-sine 11mS, 5 shocks for each of the three axes	12g, half-sine 11mS, 10 shocks for each of the three axes

Figure 14 Vibration and Shock Requirements

13 Prescribed Materials

13.1 Disallowed Components

The following components are not used in the design of the motherboard:
- Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS 6)
- Trimmers and/or potentiometers
- Dip switches

13.2 Capacitors and Inductors

The following limitations apply to the use of capacitors.
- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105C
- All capacitors have a predicted life of at least 50,000 hours at 45C inlet air temperature, under worst conditions
- Tantalum capacitors are forbidden
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes risks of cracks)
- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the design)

Only SMT inductors may be used. The use of through hole inductors is disallowed.

14   Appendix A: Detailed Power Connector Placement

The following sheet(s) contain confidential information. Do not distribute or reproduce without written permission.

Material:

FCI POWER CONNECTOR

PCI-E CONNECTOR

[2.20]
.087   MOTHERBOARD
PCB THICKNESS

A

DETAIL A
SCALE 4 : 1

[2.40]
.094   BOTTOM OF MOTHERBOARD
TO BOTTOM OF CONNECTOR

[0.20]
.008   mylar or equivalent
spacer beneath connector

[2.20]
.087   REF MOTHERBOARD PCB
THICKNESS

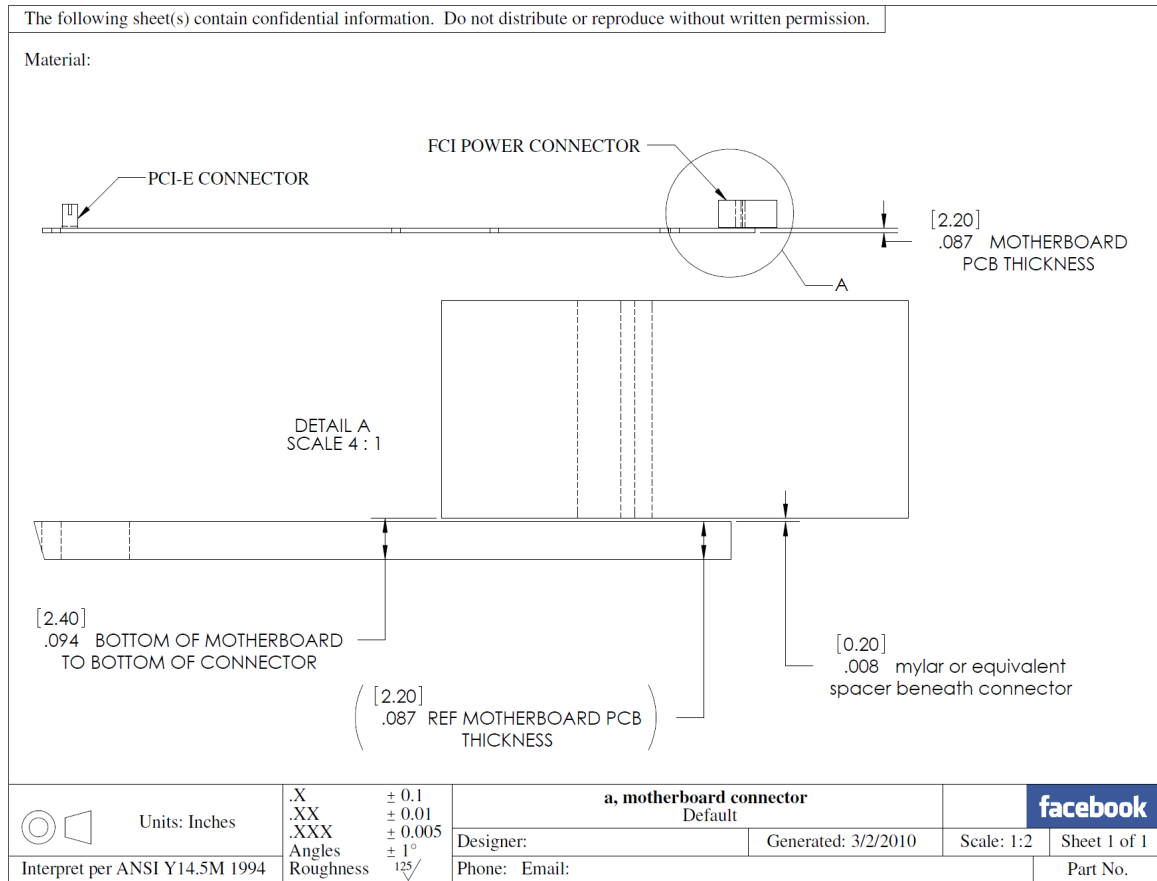| | | .X | ± 0.1 | **a, motherboard connector** | | | facebook |
	Units: Inches	.XX	± 0.01	Default			
		.XXX	± 0.005	Designer:	Generated: 3/2/2010	Scale: 1:2	Sheet 1 of 1
		Angles	± 1°				
Interpret per ANSI Y14.5M 1994	Roughness	125		Phone: Email:			Part No.

Figure 15 Detailed Power Connector Placement